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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/716,772	11/19/2003	Jose Luis Pontes Corrcia Neves	FIS920030387US1	6143

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INTERNATIONAL BUSINESS MACHINES CORPORATION
DEPT. 18G
BLDG. 300-482
2070 ROUTE 52
HOPEWELL JUNCTION, NY 12533

EXAMINER	
DOAN, NGHIA M	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 07/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/716,772	NEVES ET AL.	
	Examiner	Art Unit	
	Nghia M. Doan	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15 and 17-21* is/are rejected.

7)☒ Claim(s) *16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 November 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/19/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Responsive to communication application filed on 11/19/2003, claims 1-21 are pending.

Drawings

2. The drawings are objected to because figure 2 has an edge (D-F) containing both solid and dotted lines. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement-drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claims 1, 5, and 18 are objected to because of the following informalities: Examiner suggests that a term " critical" should be added into claims before "path associated" to make the claims cleared. .

4. Claim 16 is objected to since it is not sure whether the claim is depending on claim 1 or claim 12. Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Greidinger et al. (Greidinger) (US 6,449,761).

7. **With respect to claims 1, 12, 18 and 20**, Greidinger discloses a method (col. 3, ll. 25-26) and a computer-readable storage medium having stored therein instructions (program code) for performing a method for optimizing design (col. 3, ll. 57-60) of a microelectronic circuit using a plurality of processors (claim 14), the design having a plurality of timing paths, a subset of the timing paths being characterized as critical paths, each of the timing paths having an endpoint (fig. 10A-10C and claim 14), the method comprising the steps of:

constructing a list (file) of the critical paths (fig. 10A, 10C, elements 1050 and 1052; and col. 12, ll. 56-67) ;

constructing an endpoint (node or termination point) graph from the list of critical paths (fig. 10A, 10C; critical path 1050 contains endpoint 1002; and critical path 1052 contains endpoint 1002; and col. 11, ll. 30-52) the endpoint graph having at least one vertex representing critical paths associated with a given endpoint (fig. 10A-10C; critical paths 1050 and 1052 associated with a given endpoint 1002 having a vertices (cells) (320A, 322A, 324A, 326A, and 328A; col. 11, ll. 40-52)

partitioning (edge cut) the endpoint graph (fig. 11A-11C and col3, ll. 33-36; col. 14, ll. 24-33) in accordance with predetermined rules (col. 8, ll. 1-15) regarding timing independence and geometric (area) independence of the critical paths (col. 7, ll. 34-57; and fig. 14A-14D), thereby defining sub-sets of vertices of the endpoint graph (col. 20, ll. 17-42); and

optimizing timing of the critical paths (fig. 13 and fig. 14A-14D), said optimizing including the steps of

identifying the endpoints represented by the vertices (cells) in a given sub-set of vertices (fig. 10A-10C; col. 3, ll. 30-36; and col. 11, ll. 40-52),

identifying all critical paths ending at said identified endpoints (fig. 10A-10C, col. 3, ll. 30-32; and col. 13, ll. 9-17),

generating design changes (removing and replacing) in the microelectronic circuit to optimize said identified critical paths (col. 3, ll. 37-41 ; col. 13, ll. 25-30; and col. 14, ll. 1-13), and

storing said design changes in a memory unit (fig. 3, --initial layout S(0) change design to get final solutions S(n) and stored into memory unit -- fig. 13 and fig. 14A-D – store solution in list, which is in a memory--) ,

wherein the microelectronic circuit includes a multiplicity of components (cell/sub-cell or components/sub-components), and said method is performed after placement of the components in the design (fig. 3, col. 6, ll. 8-28; fig. 13 – process performed after placement step 1302 -- and fig. 14A-14D – more detail for fig. 13).

8. **With respect to claims 2 and 19**, Greidinger discloses all the limitations of claim 1 and 18, respectively, further discloses:

said step of constructing the set of endpoints (fig. 10A-10C, endpoints 1000, 1002) comprises constructing an endpoint graph from the list of critical paths (fig. 10A-1C, critical paths 1050, 1052), the endpoint graph having at least one vertex representing critical paths associated with a given endpoint (fig. 10A- 10C; and components 320A, 322A, 324A, 326A, and 328A; col. 11, ll. 40-52; and

said partitioning (edge cutting) step comprises partitioning the endpoint graph to define sub-sets of vertices (fig. 11 A-11C).

9. **With respect to claim 3**, Greidinger discloses a method according to claim 1, wherein the rule regarding timing (fig. 1, elements 102, 104, and 106; and col. 5, ll. 5-9) independence requires that all critical paths associated with a given endpoint are assigned to a same sub-set of paths, so that all critical paths associated with a given endpoint are optimized using a same processor (col. 8, ll. 54-64 ; and claim 14, 17 and 20).

10. **With respect to claim 4**, Greidinger discloses a method according to claim 1, wherein the rule regarding geometric (fig. 1, elements 102, 104, and 106; and col. 5, ll. 5-9) independence requires that all overlapping (saturated) critical paths are assigned to

a same sub-set of paths, so that all overlapping critical paths are optimized using a same processor (col. 8, ll. 54-64 ; and claim 14, 17 and 20)..

11. **With respect to claim 5**, Greidinger discloses a method according to claim 2, wherein the endpoint graph has at least one edge connecting two vertices (critical path 1052 and endpoint 1002 have edges E3, E6, E8, and E9, connected vertices BOT1000, 326A, 322A, and TOP1002), the edge representing overlap (saturated) between paths associated with endpoints represented by the respective two vertices (326A and 328A are overlapping).

12. **With respect to claim 6**, Greidinger discloses a method according to claim 5, wherein

said partitioning step is performed in a plurality of iterations (fig. 13, -- return path 1362 -- ; col. 19, ll. 52-57; col. 20, ll. 8-16);

in a given iteration, a vertex belonging to a given sub-set does not belong to any other sub-set (fig. 10 C and 11C); and

vertices belonging to distinct sub-sets are not connected by an edge (Fig. 11A-11C).

13. **With respect to claim 7**, Greidinger discloses a method according to claim 1, wherein said partitioning step and said optimizing step are performed in a plurality of iterations, so that critical paths not meeting said predetermined rules in a first iteration are not optimized in the first iteration (fig. 13, steps 1334, 1336 and 1360).

14. **With respect to claim 8**, Greidinger discloses a method according to claim 7, further comprising the steps of:

determining a number of iterations needed to optimize the design (fig. 13 and fig. 14B, step 1328, -- step 1330 determine number of solution required); and

determining a number of processors needed in each iteration, such that a maximum possible number of critical paths is equally balanced between processors (claim 14).

15. **With respect to claim 9**, Greidinger discloses a method according to claim 2, wherein said partitioning step and said optimizing step are performed in a plurality of iterations, so that critical paths not meeting said predetermined rules in a given iteration are not optimized in that iteration (fig. 13, steps 1334, 1336 and 1360), and

in a subsequent iteration of said partitioning step, said partitioning comprises constructing a remnant graph having vertices representing endpoints of non-optimized critical paths (as fig. 10A shown non-critical path, which is dotted lines, when performing a edge cuts at fig. 11A eliminated that non-critical path. The remnant graph having vertices representing endpoints of non- optimized path was inherent from fig. 10A-10C and fig. 11A-11C).

16. **With respect to claim 10**, Greidinger discloses a method according to claim 2, further comprising the step, prior to constructing the endpoint graph (fig. 10A, 1000, and 1002), of constructing a graph of the critical paths (fig. 10A, 1050 and 1052) characterized as a cluster graph (fig. 10A, E1,E5, E9 and E3, E6, E8, E10) the cluster graph having vertices where each vertex represents a plurality of connected critical paths (fig. 10A, 324A, 320A and 326A, 328A, 322A).

17. **With respect to claim 11**, Greidinger discloses a method according to claim 10, wherein the cluster graph has at least one edge connecting two vertices, the edge

representing overlap between areas occupied by paths represented by the respective vertices (fig. 10A, edge E6 connected vertices 326A and 328A, which are overlapping).

18. **With respect to claims 13 and 21**, Greidinger discloses all the limitations of claim 12 and 20, respectively, further discloses: wherein said optimizing is performed in parallel by the respective processors, each processor optimizing critical paths associated with a different sub-set of vertices of the endpoint graph (claim 14), so that the design changes are stored in a plurality of memory units (col. 6, ll. 38-49), and further comprising the step of updating a main memory (col. 6, ll. 38-49) by storing therein the design changes in the respective memory units after completion of optimization by all the processors (claim 14).

19. **With respect to claim 14**, Greidinger discloses a method according to claim 13, wherein said optimizing and said updating are performed in a plurality of iterations (fig. 13, -- return path 1362 -- ; col. 19, ll. 52-57; col. 20, ll. 8-16; and fig. 13, steps 1334, 1336 and 1360).

20. **With respect to claim 15**, Greidinger discloses a method according to claim 13, further comprising the step of evaluating results (solution) of said optimizing by performing a timing analysis of the critical paths (fig. 1, col. 5, ll. 1-9; and fig. 13, and 14D, step 1396-1402).

21. **With respect to claim 17**, Greidinger discloses a method according to claim 12, respectively, wherein each of the timing paths has an arrival time for a signal on that path, and a critical path is characterized (compared) as having an arrival time greater than a required arrival time (col. 7, ll. 54-63 and col. 13, ll. 55-67).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nghia M. Doan whose telephone number is 571-272-5973. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nghia M. Doan
Patent Examiner
AU 2825
NMD

VUTHE SIEK
PRIMARY EXAMINER